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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,120	09/24/2003	Mike Cogdill	200207752-1	7246

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EXAMINER

JONES, STEPHEN E

ART UNIT PAPER NUMBER

2817

DATE MAILED: 06/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/671,120

Applicant(s)

COGDILL ET AL.

Examiner

Stephen E. Jones

Art Unit

2817

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 June 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-17 and 19 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-17 and 19 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/16/05 has been entered.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-5, 7, 8, 10-12, 15-17, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buuck et al. in combination with Chi (both of record) for the reasons of record.

Buuck (Fig. 2) teaches a transmission line system including: a plurality of receiving devices; a clock signal driver (10) controlling a plurality of devices connected to the line at equal lengths from a distribution point (Claims 10, 11, 17, 19); reflections are attenuated (i.e. overshoot is managed in the same manner as the present invention since reflections are canceled) (Claim 16); and the signals are received concurrently (e.g. see Col. 2, lines 22-26) (Claim 19). Also, note that the circuit is capable of being in an integrated circuit in the same manner as the present invention, especially since it is the same as the presently claimed structure.

However, Buuck does not teach a termination (Claims 8, 15) stub that is resistive (Claim 1), including a voltage divider having the particulars of Claims 2, 3, 4, 5, 7, 16.

Chi (Fig. 5) teaches a transmission line including: a termination stub having a series resistance and a resistance to ground (i.e. termination voltage, and voltage divider) a driver (V_0); a stub matching system (i.e. a reflection dampening system) formed from a series resistance and a parallel resistance (Z_s and Y_0) coupled to ground (i.e. steady state voltage) through the parallel resistance (Claims 4-5, 7, 18); a division point (Y_d) to a plurality of output path devices (i.e. receivers) ($Y_1..Y_n$) (Claim 9).

It would have been considered obvious to one of ordinary skill in the art to have included a termination resistance/divider circuit such as taught by Chi at the distribution point in the Buuck circuit, because it would have provided the advantageous benefit of more precisely reducing reflections at the load of the transmission system, thereby suggesting the obviousness of such a modification. As an obvious consequence of the modification, the combination of Buuck and Chi is the same as the presently claimed structure thus as an obvious consequence would function in the same manner.

4. Claims 6 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buuck et al. and Chi as applied to claims 1 and 8 above, and further in view of Sato (all of record) for the reasons of record.

The combination of Buuck and Chi teaches a transmission line and termination as described above. However, they do not explicitly teach the particular resistance means or that the resistance means is a trace resistance and the paths are traces in a circuit board.

Sato provides the general teaching of forming a termination resistance and transmission path as (microstrip) traces, and as would have been well-known in the art providing an additional dielectric layer on top of the traces forms a well-known stripline structure.

It would have been considered obvious to one of ordinary skill in the art to have made the combination of Buuck and Chi circuit as a trace circuit (such as taught by Sato) formed as microstrip or stripline, because it would have been considered a well-known art-recognized equivalent/alternative transmission line system means for forming a terminated circuit.

5. Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buuck et al. and Chi as applied to claims 8 and 10-12 above, and further in view of Feraud et al. (all of record) for the reasons of record.

Buuck and Chi teach a terminated transmission line having driver clock signals (i.e. control signals) as described above, but do not explicitly teach the specific load devices are memory components/chips.

Feraud teaches a similar transmission line system that is controlled by clock signals in which the load devices (i.e. receivers) can be memory chips (e.g. see Col. 1, lines 10-16 and lines 51-55).

Accordingly, it would have been considered obvious to one of ordinary skill in the art to have the generic load devices in the combination of Buuck and Chi to have been memory cards such as taught by Feraud, because it would have been a mere selection of well-known specific load devices based on the desired use of the transmission line system.

Response to Arguments

3. Applicant's arguments filed 6/16/05 have been fully considered but they are not persuasive.

Applicant argues that Buuck teaches away from using terminations by indicating a terminator (50) (Fig. 1) is removed from the system of Fig. 2.

Applicant's argument is not persuasive. Buuck merely teaches that the Fig. 2 structure tends to cancel reflections, and nowhere in the reference does Buuck teach to not to use terminations. Also, it appears that applicant is comparing Buuck Fig. 1 to Fig. 2 to conclude that Buuck is teaching away from using terminations. However, Buuck Fig. 1 is a very different circuit from Fig. 2 in that Fig. 1 is a series device connected circuit whereas Fig. 2 is a parallel connected circuit. Furthermore, Buuck merely states that the Fig. 2 structure tends to cancel reflections. Since impedance matching (i.e. reduction of reflections) is never absolute, and what is an acceptable amount of reflections for the circuit performance is what the circuit designer must consider, the precision/degree of the reflection reduction can be more precisely controlled as stated in the rejections with Chi. Also, it should be noted that one could easily have alternatively chosen to modify the Chi reference in view of Buuck to have the device signal paths the same length.

Applicant also argues that Chi does not show a resistor in series with an input signal path and a second resistor in parallel with the input, that Fig. 5 of the Chi reference shows the ground and input path coupled in parallel to both Z_s and Y_o , and that Chi teaches away from equal length paths since Chi teaches unequal signal paths. Also, Applicant argues the combination of Chi and Sato.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections

are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

With respect to Chi, Applicant appears to be arguing the references piecemeal. It is the combined teachings which formulate the rejections. Also, it should be noted that the line connected to ground in Fig.5 of Chi is merely showing the grounded outer conductor of a coaxial line. The resistor Z_s shown in Fig. 5 is in series to the signal line and not parallel to anything except the termination resistor (Y_o) that is terminated to ground (in the same manner as the present invention).

Also, It should noted that when a particular embodiment is taught by a reference it does not mean that it "teaches away" from other arrangements.

Furthermore, Applicant argues that Feraud does not teach receivers capable of operating in an IC with control signals that control memory components.

This argument is not convincing since the present claim language merely requires the device to be capable of functioning in an IC. Furthermore, Feraud clearly teaches clock signal controls (i.e. chip select signals since the clock signals control the selection of the chip operation as is conventional).

Conclusion

All claims are drawn to the same invention claimed in the application prior to the entry of the submission under 37 CFR 1.114 and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the application prior to entry under 37 CFR 1.114. Accordingly, **THIS ACTION IS MADE**

FINAL even though it is a first action after the filing of a request for continued examination and the submission under 37 CFR 1.114. See MPEP § 706.07(b).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

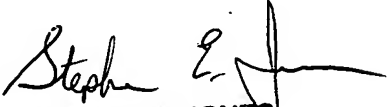
A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen E. Jones whose telephone number is 571-272-1762. The examiner can normally be reached on Monday through Friday from 8 AM to 4 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert J. Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SEJ



STEPHEN E. JONES
PRIMARY EXAMINER